AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs 57, 65, and 75 as follows:

[0057] The output 135 of the loop filter is then used to control voltage controlled oscillator ("VCO") 140. The output 145a of VCO 140 is then fed back to timing error detector 120~~a~~ to correct for any timing errors, with output 145b being the ultimate corrected output capable of driving, for example, the timing of an A-D converter such as element 50 shown in Fig. 2.

[0065] Reconstructed signal "yh" is delayed by delay circuit 330 and then, with reconstructed signal ~~and~~ "yhs," ~~are~~ compared at comparator 340, wherein if the signals are equal, comparator 340 issues a logic level of "0" as an output. If the signals are not equal, comparator 340 issues a logic level of "1" as an output. The output of comparator 340 is fed to selector 360.

[0075] The output of multiplier 240 is delayed by delay circuit 370 ~~and this is then inverted and fed to adder 320~~. At selector 360, there are three inputs: ~~the output of adder 320~~ the output of delay circuit 370, the selectable input 350, and the output of comparator 340. The output of comparator 340 determines which of the inputs to the selector 360 are passed as tha output of the selector. That is, in one example, if a logic level of "1" has been received from comparator 340 to the selector 360, then the output of adder 320 is output from selector 360. This thus subtracts any change made by the integrator circuit comprising adder 230 and multiplier 240 in relation to the signal "yh," eliminating any adjustment in the error signal produced (wherein the integrator circuit comprising elements 230 and 240 produces a gain value

by integrating data symbol signal "y" and reconstructed signal "yh"). Conversely, if the output of comparator 340 is a logic level of "0" (denoting no difference between the signals "yh" and "yhs"), then the selectable input 350 is passed as the output of selector 360. In any event, the output of selector 360 is then fed as one of the inputs to adder 280, to be combined with the output of multiplier 240.